CLAIM AMENDMENTS

1. (currently amended) A memory testing method comprising the steps of:

writing a predetermined logical value in memory cells constituting each of blocks of a memory having a block function by which memory cells in a block are erased en bloc and made rewritable;

reading out the written logical value from the memory cells in each block;

rendering a decision that, when the written logical value and the read-out logical value do not coincide with each other, such memory cell is a failure memory cell; and

~~discontinuing,~~ discontinuing the test of such block when the number of failure memory cells in a block being now tested reaches a predetermined number~~, the test of such block~~ indicating repair of the memory is impossible by substitution of spare memory components.

2. (original) The method as set forth in claim 1, further comprising the step of transferring, at the time point that the test of such block has been discontinued, a block to be tested to the next block.

3. (currently amended) The method as set forth in claim 1, further comprising the step of rendering a decision that, when the number of failure memory cells in a block being now tested reaches ~~a~~ the predetermined number, such block is to be repaired by a spare block, and wherein when such repair decision is rendered, the test of such block is discontinued.

4. (original) The method as set forth in claim 1, wherein in case a plurality of memories are concurrently tested, when a decision is rendered that a block of a memory being now tested is to be repaired by a spare block, the test of such block of the memory

is interrupted, and the test of the next block of the memory is started in synchronism with the transfer of the test of the remaining memory or memories to the next block thereof.

5. (currently amended) A memory testing method comprising the steps of:

writing a predetermined logical value in memory cells constituting each of blocks of a memory having a block function by which memory cells in a block are erased en bloc and made rewritable;

reading out the written logical value from the memory cells in each block;

rendering a decision that, when the written logical value and the read-out logical value do not coincide with each other, such memory cell is a failure memory cell; and

~~masking,~~ masking the test of memory cells on said address line in other block or blocks to be tested thereafter when the number of failure memory cells on the same address line reaches a predetermined number, ~~the test of memory cells on said address line in other block or blocks to be tested thereafter~~ indicating repair of the memory is impossible by substitution of spare memory components.

6. (original) The memory testing method as set forth in any one of claims 1 to 5, wherein when the number of blocks each being decided to be repaired by a spare block exceeds a predetermined allowable value, the memory being now tested is ended in test to be conducted thereafter.

7. (original) A memory testing apparatus for testing whether or not a predetermined logical value is correctly written in memory cells constituting each of blocks of a memory having block function, said memory testing apparatus comprising:

bad block detection and storage means detecting the presence of a failure memory cell in each block, rendering a decision that, when the number of failure

memory cells in each block reaches a predetermined number, such block is a bad block, and storing therein the result of the decision;

bad address line detection and storage means detecting the presence of a failure memory cell on the same address line, rendering a decision that, when the number of failure memory cells on the address line reaches a predetermined number, said address line is a bad address line, and storing therein the result of the decision; and

mask control means controlling to interrupt, when said bad block detection and storage means has rendered a decision that a block being now tested is a bad block, the test of the block being now tested and to write, when said bad address line detection and storage means has detected a bad address line, a forced writing signal in memory cells on the detected bad address line in the test of other block or blocks to be tested thereafter, thereby to exclude such memory cells from memory cells to be tested.

8. (original) The memory testing apparatus as set forth in claim 7, further comprising:

bad memory detecting means rendering a decision that, when it detects that a predetermined number of bad blocks has been stored in said bad block detection and storage means, the memory being tested from which such bad blocks have been generated is a bad memory; and

mask control means controlling to stop, after the time point that said bad memory detecting means has rendered a decision that the memory being tested is a bad memory, the test of the memory.